

**Remarks:**

Applicants thank Examiner Chung for her careful and patient examination of this application and the clear explanation of the claim rejections. Responding to the Office Action of January 6, 2009, Applicants reply as follows:

Claims 2-13, 16-17, and 21-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Chun et al. (US 2003/0154047). Because even in combination, the cited reference do not disclose all elements arranged as in claims 2-13, 16-17, 21-24, Applicants respectfully submit that they do not render the claims obvious.

The Office Action quotes from paragraph [0021] of Applicants' description of the invention that "[t]ypically, the test program sets hardware modules in the device tester unit for a first test, executes the first test, performs appropriate computations on the data collected by the first test, evaluates the results of the first test and then sets the hardware modules for the next test" and that "these steps are performed serially." Then the Office Action suggests that "it would have been a matter of design choice to ...program the test in serial or in parallel as desired when needed." Applicants respectfully submit that this suggestion is not based on any scientific principle or common knowledge of an artisan of mixed signal device testing.

It is well known that mixed signal testing often involves performing Fast Fourier Transforms (FFT) and this can take substantial processor time of the tester. It is also well known that testing time of a modern automated tester is very expensive. If as suggested in the Office Action that it is a matter of design choice to program the test in serial or in parallel as desired when needed, then there should be prior art references that teach such a method as arranged in the claims in this application. No such teaching is evident in any of the cited references.

The Office Action also relies on the Chun reference to disclose a tester with a special structure in which analog signals and digital signals are simultaneously handled. However, a tester that can handle analog signals and digital signals simultaneously is merely the definition of a mixed signal tester. In essence, Chun teaches a method to enhance the capability of a digital test with a "special structure" so it can handle both digital signals and analog signals, which enables the tester to test mixed signal devices. Having the capability of "handling analog and digital signals", therefore is a commonality of all mixed signal testers, and disclosing a cost effective way of enhancing the capability of a tester is very different from disclosing a method of testing a mixed signal semiconductor device as described in claim 2 and its dependent claims 3 through 11 and an apparatus as described in claim 12 and its dependent claims 13, 16, 17, and 21 through 24.

In summary, because the cited references do not disclose all the elements as arranged in the claims, Applicants respectfully submit that the claims stand distinguishable over the references and therefore stand patentable. Applicants respectfully request further examination of this application in light of the reasons presented above and timely allowance of all pending claims.

Respectfully submitted,  
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